(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 249 842 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
16.10.2002 Bulletin 2002/42

(51) Int Cl.[7]: **G11C 16/12**

(21) Application number: **01830247.1**

(22) Date of filing: **10.04.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Gregori, Stefano**
  27020 Torre d'Isola (IT)
- **Micheloni, Rino**
  22078 Turate (IT)
- **Pierin, Andrea**
  26813 Graffignana (IT)
- **Khouri, Osama**
  20146 Milano (IT)
- **Torelli, Guido**
  27016 Sant'Alessio Con Vialone (IT)

(74) Representative: **Cerbaro, Elena, Dr. et al**
STUDIO TORTA S.r.l.,
Via Viotti, 9
10121 Torino (IT)

(54) Method for programming nonvolatile memory cells with program and verify algorithm using a staircase voltage with varying step amplitude

(57) Described herein is a method for programming a nonvolatile memory cell (1), which envisages applying in succession, to the gate terminal (2) of the memory cell (1), at least a first and a second programming pulse trains (F1, F2) with pulse amplitude increasing in staircase fashion, in which the amplitude increment between one pulse and the next in the first programming pulse train (F1) is greater than the amplitude increment between one pulse and the next in the second programming pulse train (F2). Advantageously, the programming method envisages applying, to the gate terminal (2) of the memory cell (1) and before the first programming pulse train (F1), also a third programming pulse train (F0; F3) with pulse amplitude increasing in staircase fashion, in which the amplitude increment between one pulse and the next may be less than the amplitude increment in the first programming pulse train (F1) and substantially equal to the amplitude increment in the second programming pulse train (F2), or else may be greater than the amplitude increment in the first programming pulse train (F1).

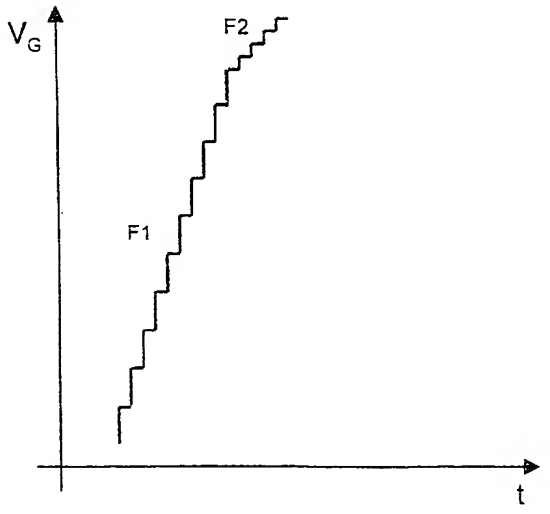


Fig.4a

EP 1 249 842 A1

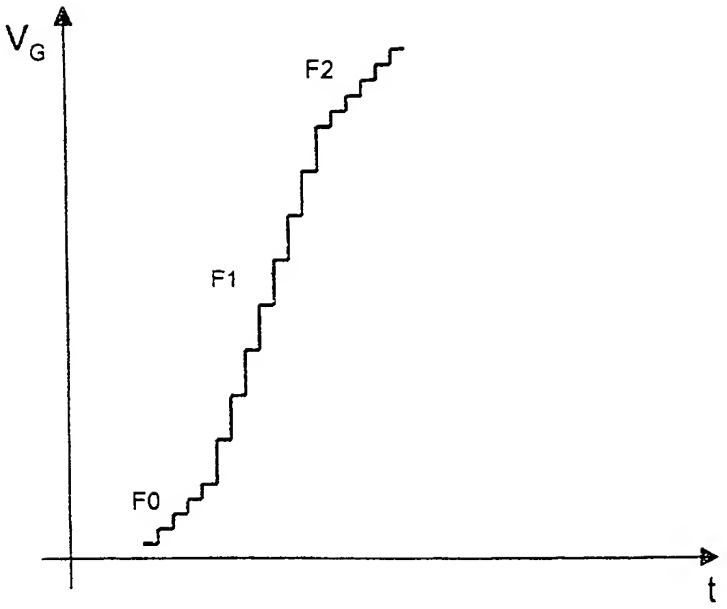


Fig.5a

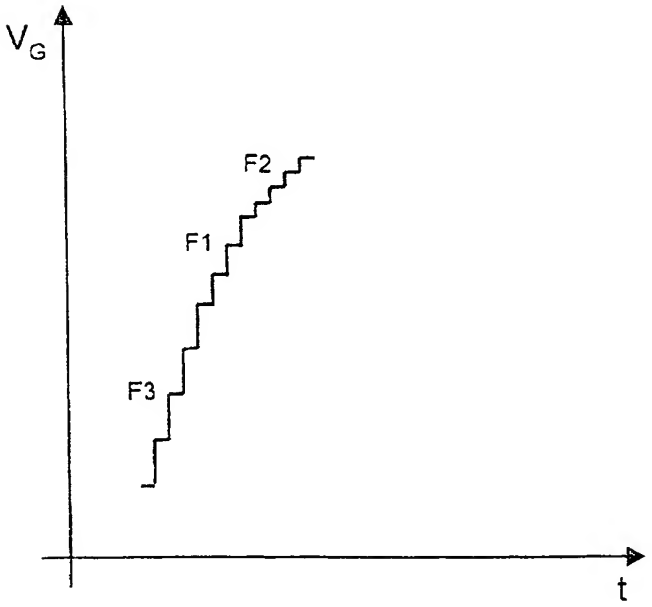


Fig.6a

Description

[0001] The present invention relates to a method for programming nonvolatile memory cells with a program and verify algorithm in which the amplitude of the programming pulses increases in staircase fashion with a variable slope.

[0002] As is known, the most widely used programming methods for nonvolatile memory cells are based upon program and verify algorithms. This approach can be applied both to programming by injection of hot electrons from the channel and to programming via Fowler-Nordheim tunnelling, and is particularly indicated whenever a high programming precision is required, as in the case of multilevel storage.

[0003] Programming of a nonvolatile memory cell is normally performed by means of a sequence of programming steps interspersed with verification steps in which the state of the memory cell is verified. In this connection, see, for example, G. Torelli, P. Lupi, "An improved method for programming a word-erasable EEPROM", *Alta Frequenza*, Vol. LII, n. 6, Nov./Dec. 1983, pp. 487-494.

[0004] In particular, during the programming steps a programming voltage is applied to the gate terminal of the memory cell, the amplitude of which is increased by a constant amount at each programming step, and the sequence is continued until the threshold voltage of the memory cell, which was initially at a low value, reaches the desired value.

[0005] In order for the programmed level of the threshold voltage to be increased by the same amount at each step, with a constant temporal duration for the programming steps, it is necessary to apply increasingly higher programming voltages to the gate terminal of the memory cell being programmed. If at each programming step the voltage V_G on the gate terminal is increased by a constant amount $\Delta V_G = V_{G,(i+1)} - V_{G,i}$ (where i designates a generic programming step) and if the temporal duration of the programming phase at each individual step is sufficient, in steady-state conditions a constant increment $\Delta V_T = V_{T,(i+1)} - V_{T,i}$ is obtained of the threshold voltage for each programming step.

[0006] In this connection, see, for example, C. Calligaro, A. Manstretta, P. Rolandi, G. Torelli, "Technological and design constraints for multilevel flash memories", *Proc. 3rd IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Oct. 1996, pp. 1005-1008, and T.S. Jung, *et al.*, "A 17-mm2 3.3 V only 128-Mb multilevel NAND Flash memory for mass storage applications", *IEEE J. Solid-State Circuits*, vol. 31, No. 11, 1996, pp. 1575-1583, in which programming methods are described for programming multilevel memories with a pulsed voltage, the amplitude of which increases in staircase fashion with a constant slope, i.e., in which the programming voltage is constituted by a succession of programming pulses where the voltage difference between one pulse and the preceding one is constant.

[0007] Figure 1 shows a graph presented in the above-mentioned paper "Technological and design constraints for multilevel flash memories" and representing the linear relationship existing between the threshold voltage of a memory cell and the programming voltage applied to the gate terminal of the memory cell, when said programming voltage presents a pulsed pattern the amplitude of which increases in staircase fashion.

[0008] In particular, Figure 1 shows various programming curves obtained with ΔV_G = 500 mV, in which appearing on the top horizontal axis is the voltage V_G applied to the gate terminal of a memory cell, on the bottom horizontal axis is the number of steps, and on the vertical axis is the overall threshold-voltage variation starting from a pre-set initial value (in Figure 1, ΔV_T designates the overall threshold-voltage variation, whereas in the present text ΔV_T designates the threshold-voltage variation obtained with a single programming pulse).

[0009] When a program and verify algorithm is used, the amplitude of the programmed threshold voltage distributions depends upon the variation of the threshold voltage ΔV_T obtained at each step. In particular, the programming precision, i.e., the maximum difference between the threshold-voltage value actually obtained and the desired nominal value, depends upon ΔV_T. For practical purposes, therefore, the programming precision depends upon ΔV_G, i.e., upon the increment of the programming voltage at each programming step.

[0010] In order to obtain a high programming precision, which is indispensable in multilevel digital storage, it is thus necessary to reduce ΔV_G as much as possible. In this connection, see, for example, B. Riccò, *et al.*, "Nonvolatile multilevel memories for digital applications", *Proceedings of the IEEE*, Vol. 86, No. 12, Dec. 1998, pp. 2399-2421.

[0011] Obviously, the higher the number of bits that are to be stored in the individual memory cell, the greater is the programming precision required. If the same range of programmable threshold voltages is available, given the same technological generation, in order to increase by one bit the information content storable in a single cell, it is necessary at least to double the programming precision. For practical purposes, even when the programming precision is doubled, the noise margin between two adjacent distributions of programmed threshold voltages is halved, and hence the programming precision must be further increased in order to obtain an acceptable level of reliability.

[0012] Figure 2 is a qualitative representation of the distributions of programmed threshold voltages for multilevel cells with 2-bit per cell, using a technology currently available in which the range of programmable threshold voltages is fixed between 1 V and 6 V. Also represented in Figure 2 are the distributions of threshold voltages that may be obtained in the same voltage range for multilevel cells with 4-bit per cell. Likewise represented in Figure 2, as hatched areas, are the corresponding noise margins.

[0013] In this case, even supposing that it is possible to reduce the noise margins by a factor of four, the width of the programmed threshold voltage distributions must be reduced by at least a factor of four.

[0014] Reduction in ΔV_G in order to increase programming precision determines an increase in programming times. To obtain the same overall threshold voltage variation, using programming steps having the same temporal duration, with ΔV_G halved, twice as much time is required. Returning to the previous example, given the same technology, 4-bit-per-cell programming, as compared to 2-bit-per-cell programming, requires at least four times as long. For this reason, the increase in programming times may prove a limit for the development of multilevel memories with a high number of bits per cell.

[0015] In order to reduce the programming time, then, programming methods have been proposed for programming nonvolatile memories with staircase programming voltages,
where the amplitude of the steps is not constant, but rather varies according to different modalities.

[0016] For example, the US patents US-A-4,357,685 "Method of programming an electrically alterable nonvolatile memory", and US-A-5,812,457 "Semiconductor NAND type flash memory with incremental step pulse programming" describe methods for programming non-multilevel memories, in which the programming voltage is formed by a succession of programming pulses having increasing amplitude or duration, whilst the US patent US-A-5,257,255 "Method for programming programmable devices by utilizing single or multiple pulses varying in pulse width and amplitude" describes a programming method that uses single or multiple pulses having varying amplitude or duration, in which a first train of programming pulses is applied to an electrode of the programmable device and, simultaneously, a second train of programming pulses is applied to a second electrode of the programmable device.

[0017] Although the programming methods using staircase programming voltages with varying incremental amplitude between adjacent programming steps described in the aforementioned patents enable a reduction in the time for programming nonvolatile memories as compared to programming methods using staircase programming voltages in which the increment in amplitude between adjacent programming steps (i.e., between one programming step and the next) is constant, they currently form the subject of continuous study and research in so far as the effective reduction in the programming time that they make possible is not yet altogether satisfactory.

[0018] The purpose of the present invention is to provide a method for programming nonvolatile memory cells with a staircase programming voltage having varying incremental amplitude between adjacent programming steps, the said method being based on a program and verify algorithm that enables a further reduction in the time required for high-precision programming as compared to conventional programming methods.

[0019] According to the present invention, a method for programming a memory cell based upon a program and verify algorithm is provided, as defined in Claim 1.

[0020] For a better understanding of the present invention, some preferred embodiments thereof are now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- Figure 1 shows a graph representing the linear relationship existing between the threshold voltage of a memory cell and the programming voltage applied to the gate terminal of the memory cell, when the programming voltage presents a staircase waveform;
- Figures 2a and 2b are representations of the programmed threshold voltage distributions for multilevel cells with 2-bit per cell and, respectively, 4-bit per cell, and of the corresponding noise margins;
- Figure 3 is a schematic representation of a nonvolatile memory cell;
- Figure 4a shows, in a simplified and qualitative way, the plot as a function of time of the programming voltage applied to the gate terminal of the memory cell of Figure 1 in a first embodiment of the present invention;
- Figures 4b and 4c are the effective plots as a function of time of the voltages applied to the gate terminal and, respectively, to the drain terminal of the memory cell of Figure 1 in the first embodiment of the present invention;
- Figure 5a shows, in a simplified and qualitative way, the plot as a function of time of the programming voltage applied to the gate terminal of the memory cell of Figure 1 in a second embodiment of the present invention;
- Figures 5b and 5c are the effective plots as a function of time of the voltages applied to the gate terminal and, respectively, to the drain terminal of the memory cell of Figure 1 in the second embodiment of the present invention;
- Figure 6a shows, in a simplified and qualitative way, the plot as a function of time of the programming voltage applied to the gate terminal of the memory cell of Figure 1 in a third embodiment of the present invention;
- Figures 6b and 6c are the effective plots as a function of time of the voltages applied to the gate terminal and, respectively, to the drain terminal of the memory cell of Figure 1 in the third embodiment of the present invention;
- Figures 7, 8 and 9 are tables referring to the programming method according to the present invention;
- Figures 10a and 10b show, respectively, a plot as a function of time of the programming voltage applied to the gate terminal of a memory cell with voltage increment between adjacent steps that assumes two possible values, and a plot as a function of time of the corresponding programmed threshold voltage;
- Figure 11 shows the a switched-capacitor circuit for the generation of a varying incremental staircase voltage; and
- Figure 12 shows the block diagram of a circuit for the generation of the staircase programming voltage with varying increments between adjacent steps.

[0021] Figure 3 shows a nonvolatile memory cell 1 to be programmed that forms part of a nonvolatile memory device, in which the gate terminal is designated by 2, the drain terminal by 4, and the source terminal by 6.

[0022] In particular, as is known, in a nonvolatile memory device the gate terminal 2 of a memory cell is connected to an array row (not shown) selectable by means of a row decoder (not shown), the drain terminal 4 is connected to an array column (not shown) selectable by means of a column decoder (not shown), whilst the source terminal 6 is connected to a common line (not shown).

[0023] The inventive principle lying at the basis of the present invention will be described in what follows with reference to Figures 4, 5 and 6, which show the plots as a function of time of the programming voltage V_G and of the voltage V_D respectively applied to the gate terminal 2 and to the drain terminal 4 of the memory cell 1, in three different embodiments of the present invention.

[0024] In particular, Figure 4a shows the staircase waveform of the amplitude of the programming voltage V_G applied to the gate terminal of the memory cell 1 in the first embodiment of the present invention.

[0025] In actual fact, the staircase programming voltage V_G is not formed by a series of voltage steps succeeding one another in time, but rather of a series of voltage pulses of progressively increasing amplitude succeeding one another in time, as shown in Figure 4b.

[0026] Figure 4c is instead the plot as a function of time of the voltage V_D applied to the drain terminal 4 of the memory cell 1, again in the first embodiment of the present invention.

[0027] In particular, as shown in Figures 4a-4c, the first embodiment of the invention envisages programming of the memory cell 1 in two phases.

[0028] In the first phase, designated in the figure by F1 to the drain terminal 4 and to the gate terminal 2 of the memory cell 1 to be programmed there is applied a first pair of programming (voltage) pulse trains; namely, one programming pulse train of the pair is applied to the drain terminal 4, and the other to the gate terminal 2. The programming pulses applied to the drain terminal 4 (V_D) have a constant amplitude, for example of between 4 V and 5 V, whereas the programming pulses applied to the gate terminal 2 (V_G) have an increasing amplitude, in such a way that the voltage difference between one programming pulse and the preceding one, i.e., the voltage increment between adjacent pulses ΔV_{G1}, is constant and has a high value, in particular higher than the precision desired for the programmed threshold voltage, for example a value of between 200 mV and 600 mV.

[0029] In the second phase, instead, designated in the figure by F2, to the drain terminal 4 and to the gate terminal 2 of the memory cell 1 to be programmed there is applied a second pair of programming pulse trains; namely, one programming pulse train of the pair is applied to the drain terminal 4, and the other to the gate terminal 2. The programming pulses applied to the drain terminal 4 (V_D) again have a constant amplitude, preferably equal to the one in the first phase F1, whereas the programming pulses applied to the gate terminal 2 (V_G) have an increasing amplitude, in such a way that the voltage difference between one programming pulse and the preceding one, i.e., the voltage increment between adjacent pulses ΔV_{G2}, is again constant but has a value lower than ΔV_{G1} and is of the same order of precision as that desired for the threshold voltage programmed, for example between 50 mV and 100 mV.

[0030] In addition, the first programming pulse of the second programming pulse train applied to the gate terminal 2 of the memory cell 1 in the second phase F2 has an amplitude equal to that of the last programming pulse of the first programming pulse train applied to the gate terminal 2 in the first phase F1 increased by a quantity ΔV_{G2}.

[0031] Furthermore, transition from the first phase F1 to the second phase F2 takes place after the threshold voltage V_T of the memory cell 1 has exceeded a pre-set reference value V_{TR1}, appropriately chosen below the value of the threshold voltage at which the memory cell 1 is to be programmed.

[0032] Figures 5a, 5b and 5c are similar to Figures 4a, 4b and 4c and show the plots as a function of time of the programming voltage V_G and of the voltage V_D respectively applied to the gate terminal 2 and to the drain terminal 4 of the memory cell 1 in the second embodiment of the present invention.

[0033] In particular, as shown in Figures 5a-5c, the second embodiment of the present invention envisages programming of the memory cell 1 in three phases.

[0034] In the first phase, designated in the figure by F0, to the drain terminal 4 and to the gate terminal 2 of the memory cell 1 to be programmed there is applied a first pair of programming pulse trains; namely, one programming pulse train of the pair is applied to the drain terminal 4, and the other to the gate terminal 2. The programming pulses applied to the drain terminal 4 have a constant amplitude, for example preferably equal to the one applied in the phases F1 and F2 of the first embodiment, whereas the programming pulses applied to the gate terminal 2 have an increasing amplitude, in such a way that the voltage difference between one programming pulse and the preceding one, i.e., the voltage increment between adjacent pulses ΔV_{G0}, is constant and has a limited value, for example of the same order as that of the precision desired for the programmed threshold voltage.

[0035] In the first phase F0, the memory cells with different starting threshold voltages or with different characteristics due to the process spreads are substantially brought back to the same conditions.

[0036] The two subsequent phases are the same as the phases F1 and F2 of the first embodiment, and consequently will not be described again.

[0037] It is only emphasized that ΔV_{G0} may also be equal to ΔV_{G2}, and that the first pulse of the second phase (phase F1) has an amplitude equal to that of the last pulse of the first phase (phase F0) increased by a quantity ΔV_{G1}.

[0038] Transition from the first phase F0 to the second phase F1 can take place after a fixed number of pulses, or else after the threshold voltage V_T of the memory cell 1 has exceeded an appropriately chosen pre-set reference value V_{TR0}.

[0039] Transition from the second phase F1 to the third phase F2 takes place in a way identical to what was described for the first embodiment.

[0040] Figures 6a, 6b and 6c are similar to Figures 4a, 4b and 4c and show the plots as a function of time of the programming voltage V_G and of the voltage V_D respectively applied to the gate terminal 2 and to the drain terminal 4 of the memory cell 1 in a third embodiment of the present invention.

[0041] In particular, as shown in Figures 6a-6c, the third embodiment of the present invention represents one of the possible variants of the second embodiment and differs from the latter in that the first programming pulse train applied to the gate terminal 2 of the memory cell 1, designated in the figure by F3, presents a voltage increment between adjacent pulses greater than the one present in the programming pulse train applied to the gate terminal 2 in the second phase F1.

[0042] In other words, the third embodiment envisages that programming of the memory cell 1 takes place always in three phases, but that a phase F1 is used with a voltage increment between adjacent pulses that is intermediate between the initial phase F3, in which said increment is greater, and the end phase F2, in which said increment is smaller.

[0043] In addition, it is also possible to use a series of intermediate phases with a voltage increment between adjacent pulses that is progressively decreasing in amount so as to obtain the most satisfactory compromise between programming precision and programming time.

[0044] From what has been described above it is evident that, unlike what is proposed in the documents of the prior art, and in particular in the US patent US-A-5,257,255, the present invention proposes a method in which programming of a memory cell is performed by means of application, to a first terminal of the memory cell, namely the gate terminal in the case of memories programmed by injection of channel hot electrons, of at least two distinct successive trains of voltage pulses having precise characteristics, where each train presents pulses in which the voltage is incremented by a given constant value between one pulse and the next, and the value of this increment is different for the different pulse trains, whilst to a second terminal of the memory cell, namely the drain terminal in the case of memory cells programmed by injection of channel hot electrons, there are applied pulse trains having a substantially constant amplitude simultaneously with the pulse trains applied to the gate terminal which have been described previously.

[0045] Transition from one pulse train to another (with the possible exclusion of the transition from phase F0 to phase F1 in the second embodiment) does not follow any pre-defined procedure, but takes place according to the result of the verify operation, which is performed at each programming step by using appropriate references.

[0046] The advantages that may be achieved with the programming methods according to the present invention in terms of memory cell programming speed will emerge clearly from what follows.

[0047] Suppose that during a programming pulse with constant drain, source and substrate voltages, the gate current I_G is an increasing function of V_G - V_T:

$$I_G = f(V_G - V_T) \tag{1}$$

The gate current I_G is linked to the charge Q_{FG} stored in the floating gate, and hence to the threshold voltage V_T, by the following relation:

$$I_G = -\frac{dQ_{FG}}{dt} = C_G\frac{dV_T}{dt} \tag{2}$$

where C_G is the capacitance between the floating gate and the control gate.

[0048] The differential relation that governs the variation of the threshold voltage V_T during a programming pulse is then:

$$\frac{dV_T}{dt} = \frac{f(V_G - V_T)}{C_G} \tag{3}$$

[0049] It may be noted that as the threshold voltage V_T increases there is a decrease in its time derivative dV_T/dt.

[0050] Suppose that a gate voltage V_G higher than the initial threshold voltage of the memory cell is applied, such that injection of hot electrons from the channel into the floating gate is triggered. The variation in the threshold voltage obtained in a programming step depends upon the initial difference between the voltages $V_{G,\,applied} - V_{T,initial} - V_D$, where V_D is a constant that depends upon the biasing conditions and physical characteristics of the memory cell. More precisely, if the programming pulse had an infinite duration, the variation in the threshold voltage would be equal to the value indicated. On account of the non-complete disappearance of the transient during a programming pulse, the threshold-voltage variation actually obtained is a fraction γ of the initial difference between the voltage $V_{G,applied} - V_{T,initial} - V_D$.

[0051] If a simplified model with a single time constant is used, γ depends only upon the duration of the programming pulse, the biasing voltages, and the physical characteristics of the memory cell. Consequently, if programming pulses having a constant duration are considered, γ is a constant.

[0052] If a program and verify algorithm is used with pulsed gate programming voltage with incremental staircase voltage amplitude having constant increments between adjacent pulses (as pointed out previously, with this technique at each programming pulse the gate voltage is increased by a constant quantity ΔV_G with respect to the value reached at the preceding pulse), the threshold voltage at the end of the i-th programming pulse is then given by the following relation:

$$V_{T,i} = V_{T,i-1} + \gamma\,(V_{G,i} - V_{T,i-1} - V_D) \tag{4}$$

Introducing the difference between the gate voltage and the threshold voltage at the end of the pulse:

$$X_i = V_{G,i} - V_{T,i} \tag{5}$$

and, making the substitution:

$$V_{G,i} = V_{G,0} + i\Delta V_G \tag{6}$$

we obtain:

$$X_{i+1} - X_i = ((1 - \gamma)\Delta V_G + \gamma V_D) - \gamma X_i \tag{7}$$

[0053] Equation (7) is a discrete-time differential equation of the first order, from which it is found that the steady-state value $(\Delta V_G(1 - \gamma)/\gamma + V_D)$ is reached with a constant $1/\gamma$ over the number of programming steps.

[0054] For the present purposes, if the value of the increment ΔV_G is varied, for example if there is a transition from an increment ΔV_{G1} to an increment ΔV_{G2}, adaptation on the corresponding threshold voltage variations obtained at each programming step takes place with a constant $1/\gamma$.

[0055] Suppose that after n programming steps with a programming voltage increment ΔV_{G1} between adjacent steps, in the course of which the threshold voltage variation at each pulse has reached the steady-state value, the programming voltage increment between adjacent steps is reduced to ΔV_{G2} (with $\Delta V_{G2} < \Delta V_{G1}$).

[0056] The error on the threshold voltage increment after i pulses starting from the n-th pulse is given by the following equation:

$$X_{n+i-1} - X_{n-i} = (1 - \gamma)^i\,(\Delta V_{G1} - \Delta V_{G2}) \tag{8}$$

[0057] Table I of Figure 7 gives the errors on the threshold voltage variation that is obtained after transition from an increment value ΔV_{G2} to a reduced increment value ΔV_{G1}. More precisely, the table gives the errors found after the first pulse $(n + 1)$ with reduced ΔV_G, after the second pulse $(n + 2)$, after the third pulse $(n + 3)$, and so forth.

[0058] Table II of Figure 8, instead, gives the values of the threshold voltage variation (ΔV_T) obtained in the transition from $\Delta V_{G1} = 400$ mV to $\Delta V_{G2} = 100$ mV, with different values of γ ($\gamma = 0.6$; 0.7; 0.8; 0.9) for the first ten pulses after the variation. The n-th programming pulse is the last one where an increment $\Delta V_G = \Delta V_{G1} = 400$ mV is applied, so that the corresponding threshold voltage variation ΔV_{G1} is still 400 mV. Starting from the next pulse $(n + 1)$, the increment

applied is $\Delta V_G = \Delta V_{G2} = 100$ mV. The threshold voltage variation obtained in the course of the subsequent pulses converges towards the steady-state value (100 mV).

[0059] Finally, Table III of Figure 9 gives the percentage errors on the threshold voltage variation that correspond to the previous example. It may be noted that the error, which is high at the first pulse, decreases rapidly in the subsequent pulses, whilst the threshold voltage variation converges to its steady-state value. For example, if $\gamma = 0.8$, at the second pulse the error is already only 12% with respect to the increment ΔV_G, whilst at the fourth pulse it is lower than 0.5%.

[0060] This demonstrates the possibility of reducing the programming voltage increment between adjacent programming steps, maintaining a high precision on the threshold voltage variation obtained. In particular, it is possible to pass from a phase (F1) of fast programming (ΔV_G high) to a phase (F2) of fine programming (ΔV_G reduced), obtaining an excellent correspondence between programming voltage increment and threshold voltage variation in a limited number of pulses after the transition.

[0061] An example of the programming curves that may be obtained using the present invention is represented in Figures 10a and 10b, which show the plot (10a) of the programming voltage applied to the gate terminal of a memory cell with an increment between adjacent programming steps that assumes two possible values, and the plot (10b) of the corresponding programmed threshold voltage. In this example there appear the staircase programming voltages with 200-mV (phase F1) and 50-mV (phase F2) increments between adjacent steps, which indicatively are able to provide the necessary programming precision for 2-bit-per-cell and 4-bit-per-cell storage. The temporal duration of a single program and verify step is 2 μs.

[0062] Programming with varying increments speeds up programming of the individual multilevel cell; for example, it is possible to obtain programming with the precision necessary for 16 levels in the same time that is required for 4 levels with fixed voltage increments.

[0063] To program a cell, the procedure starts with fast programming (F1) until the threshold voltage, controlled in the verify steps, reaches a value close to the one desired (V_{TR1}), and then proceeds with fine programming (F2) until the desired value is reached.

[0064] During reading, an appropriate electric quantity (voltage or current) is extracted from the multilevel memory cell and compared with a set of reference values in order to reconstruct the information content of the memory cell in terms of binary information.

[0065] During each verify step generally a complete reading of the memory cell is not performed, but simply the electric quantity extracted is compared with a single reference value, which depends upon the threshold voltage value at which the memory cell is to be programmed. To carry out this operation, one of the comparators used for reading can be utilized.

[0066] In the program and verify technique with varying incremental steps according to the present invention, the comparator used for the verification compares the value of the electric quantity extracted from the memory cell, which is linked to the threshold voltage reached, with:

- a preliminary reference, appropriately chosen lower than the target value, during fast programming; and
- the final reference, once there has been the transition to fine programming.

[0067] In order to optimize programming speed and precision, it is possible to apply programming voltages with staircase pulse amplitude also with voltage increments between adjacent programming steps that can be selected from among more than two different values, passing from the large step of fast programming to the smaller step of fine programming through a series of intermediate values, as described previously for the third programming method according to the present invention.

[0068] For generating a staircase voltage with varying increments between adjacent steps, a possible circuit implementation can be based upon the switched-capacitor circuit proposed in the US patent US-A-5949666, "Staircase adaptive voltage generator circuit" and represented for completeness of description in Figure 11, where the control signal CNT selects the amplitude of the step, and the two phases Φ_1 and Φ_2 are not superimposed.

[0069] In this circuit, the two possible increments between adjacent values are:

$$\begin{cases} \Delta V_{G1} = \dfrac{C_A + C_B}{C_F}\left(V_{init} - V_{ref}\right) & \text{fast program min g} \\ \Delta V_{G2} = \dfrac{C_B}{C_F}\left(V_{init} - V_{ref}\right) & \text{fine program min g} \end{cases} \tag{9}$$

according to whether the control signal CNT is active or not.

[0070] To obtain an increment of amplitude selectable from among more than two values, it is possible to connect selectively more than one capacitor in parallel to C_B.

[0071] Two possible alternatives to obtain the incremental variation in the programming voltage consist in connecting an additional capacitor in parallel to C_F instead of to C_B or in varying one of the two reference voltages V_{init} or V_{ref}.

[0072] Another possible circuit diagram for implementing a circuit generating a staircase voltage with digitally selectable increments is described in the Italian patent applications TO99A000993 "Voltage generator switchable between first and second voltage values alternate to one another, in particular for programming multilevel cells", and TO99A000994 "Programmable voltage generator, in particular for programming multilevel nonvolatile memory cells", where two or more alternatively selectable resistors having appropriate values are used.

[0073] The complete circuit for generating the programming voltage is formed by a staircase generator block (of the type of the ones referred to above) and possibly by an amplifier, connected in unit-gain configuration, which is capable of fast driving of the parasitic capacitance associated to the array row driving stage, as represented in Figure 12.

[0074] For high-performance multilevel memories it is possible to implement a compact staircase generating circuit, for example based upon a switched-capacitor block, with the function of programming a memory cell, alongside each voltage read circuit, an arrangement which is perfectly integratable in hierarchical decoding with digital row selection (for example, of the type described in the Italian patent application MI00A001585 "Hierarchical decoding with digital row selection for nonvolatile memory devices").

[0075] In this way, a programming parallelism can be obtained that is the same as the reading parallelism, together with the maximum versatility in the management of the programming procedure.

[0076] Finally, it is clear that modifications and variations can be made to the programming methods described and illustrated herein, without thereby departing from the sphere of protection of the present invention, as defined in the attached claims.

Claims

1. A method for programming a memory cell (1), **characterized in that** it comprises the step of applying in succession, to a control terminal (2) of said memory cell (1), at least a first and a second programming pulse trains (F1, F2) with pulse amplitude increasing in staircase fashion, in which the amplitude increment between one pulse and next in said first programming pulse train (F1) is greater than the amplitude increment between one pulse and the next in said second programming pulse train (F2).

2. The programming method according to Claim 1, **characterized in that** transition from said first programming pulse train (F1) to said second programming pulse train (F2) is made when said memory cell (1) has a threshold voltage (V_T) having a first pre-set relation with a first reference value (V_{TR1}).

3. The programming method according to Claim 2, **characterized in that** said first pre-set relation is defined by the condition that the threshold voltage (V_T) of said memory cell (1) exceeds said first reference value (V_{TR1}).

4. The programming method according to Claim 2 or Claim 3, **characterized in that** said first reference value (V_{TR1}) is correlated to the threshold voltage (V_T) at which said memory cell (1) is to be programmed.

5. The programming method according to Claim 4, **characterized in that** said first reference value (V_{TR1}) is lower than the threshold voltage (V_T) at which said memory cell (1) is to be programmed.

6. The programming method according to any of the foregoing claims, **characterized in that** it further comprises the step of applying, to said control terminal (2) of said memory cell (1) and before said first programming pulse train (F1), a third programming pulse train (F0; F3) with pulse amplitude increasing in staircase fashion.

7. The programming method according to Claim 6, **characterized in that** the amplitude increment between one pulse and the next in said third programming pulse train (F0) is less than the amplitude increment between one pulse and the next in said first programming pulse train (F1).

8. The programming method according to Claim 6 or Claim 7, **characterized in that** the amplitude increment between one pulse and the next in said third programming pulse train (F0) is substantially equal to the amplitude increment between one pulse and the next in said second programming pulse train (F2).

9. The programming method according to Claim 6, **characterized in that** the amplitude increment between one pulse

and the next in said third programming pulse train (F3) is greater than the amplitude increment between one pulse and the next in said first programming pulse train (F1).

10. The programming method according to any of Claims 6 to 9, **characterized in that** transition from said third programming pulse train (F0; F3) to said first programming pulse train (F1) is made when said memory cell (1) presents a threshold voltage (V_T) having a second pre-set relation with a second reference value (V_{TR0}).

11. The programming method according to Claim 10, **characterized in that** said second pre-set relation is defined by the condition that the threshold voltage (V_T) of said memory cell (1) exceeds said second reference value (V_{TR0}).

12. The programming method according to any of Claims 6 to 9, **characterized in that** transition from said third programming pulse train (F0; F3) to said first programming pulse train (F1) is made after a pre-set number of programming pulses.

13. The programming method according to any of the foregoing claims, **characterized in that** it further comprises the step of applying, to a first terminal (4) of said memory cell (1) and simultaneously to each one of said programming pulse trains (F0, F1, F2, F3) applied to said control terminal (2), a respective programming pulse trains (V_D) with constant pulse amplitude.

14. The programming method according to Claim 13, **characterized in that** said programming pulse trains (V_D) applied to said first terminal (4) of said memory cell (1) have pulse amplitudes substantially equal to one another.

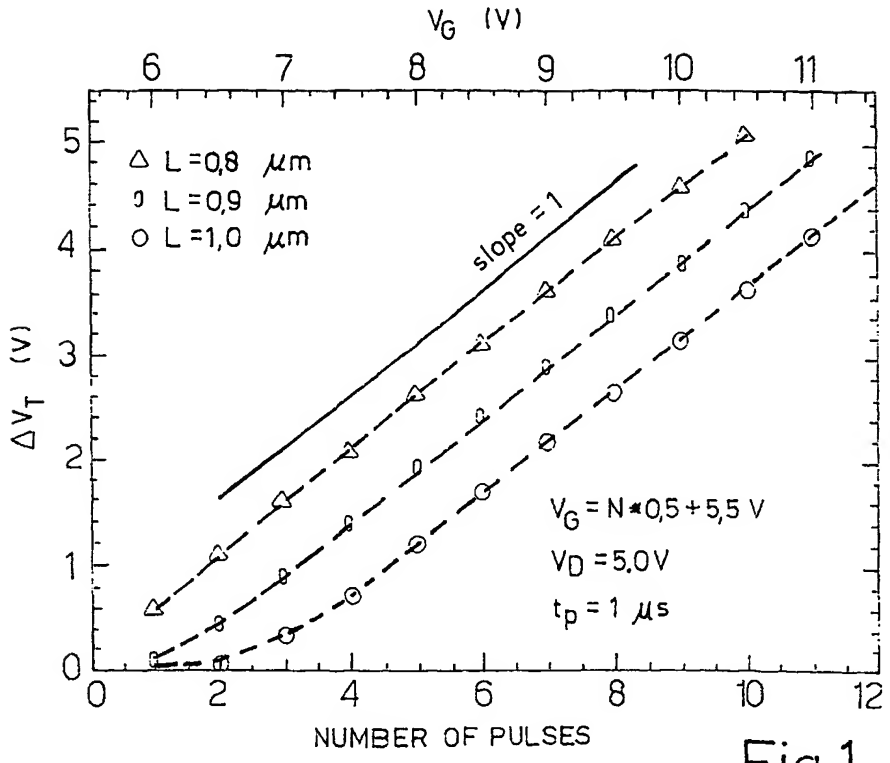


Fig.1

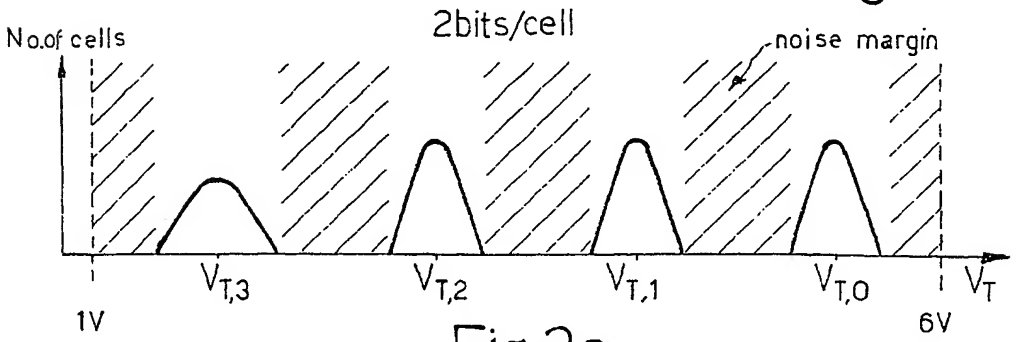
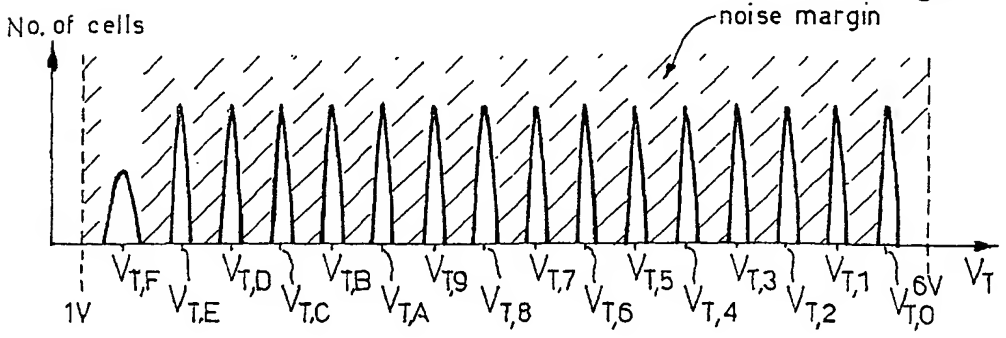


Fig.2a

Fig.2b



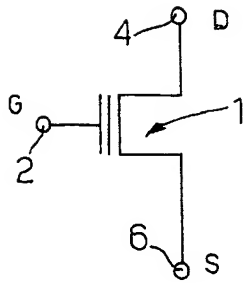


Fig. 3

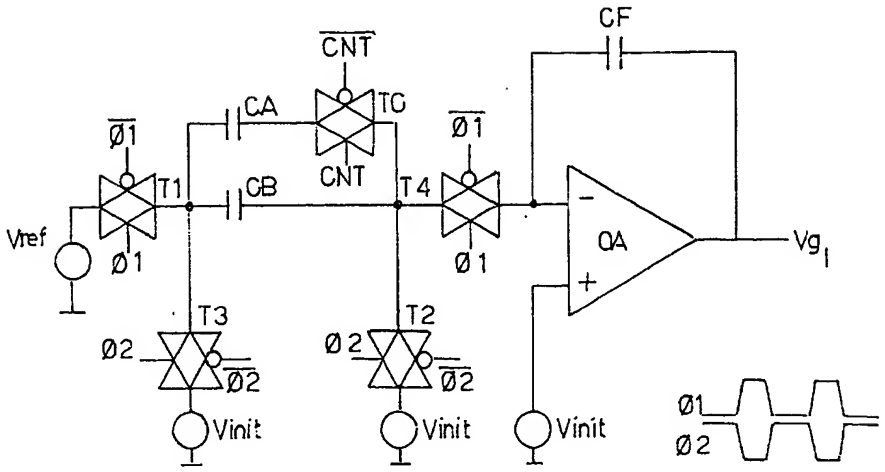


Fig.11

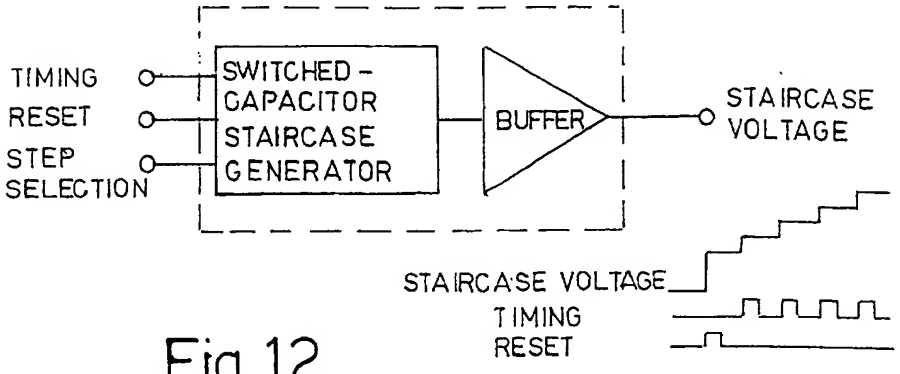


Fig. 12

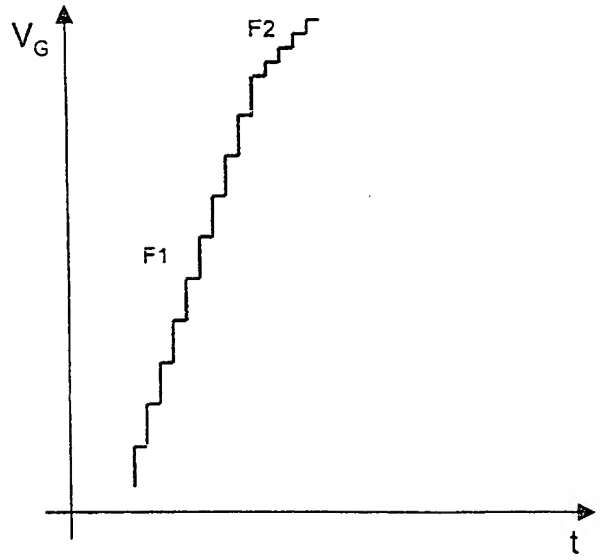


Fig.4a

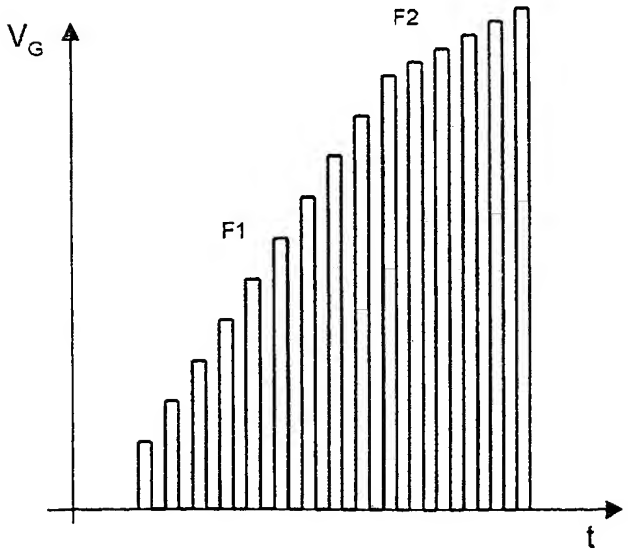


Fig.4b

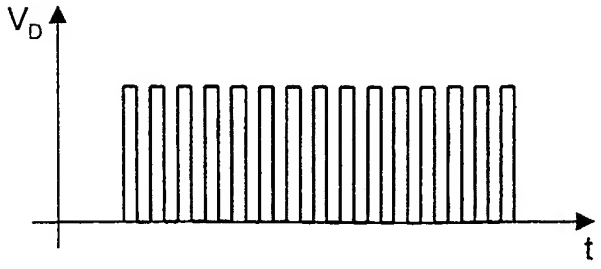


Fig.4c

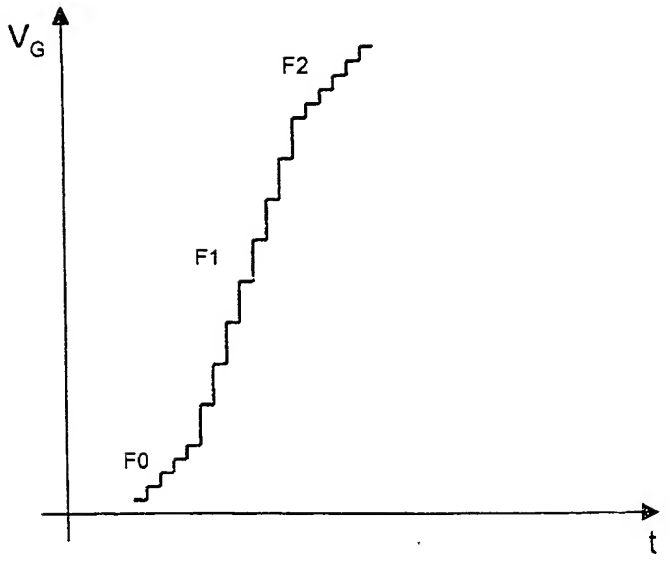


Fig.5a

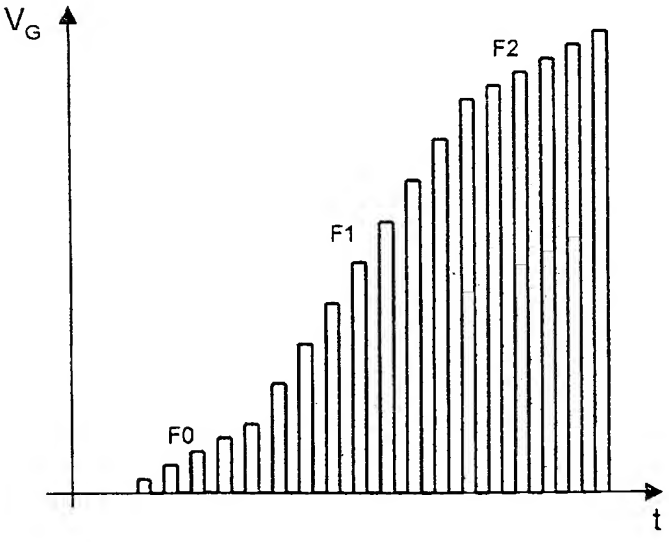


Fig.5b

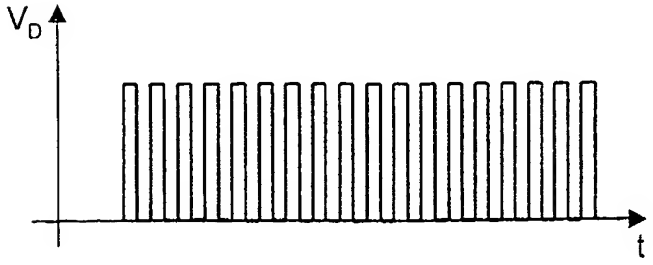


Fig.5c

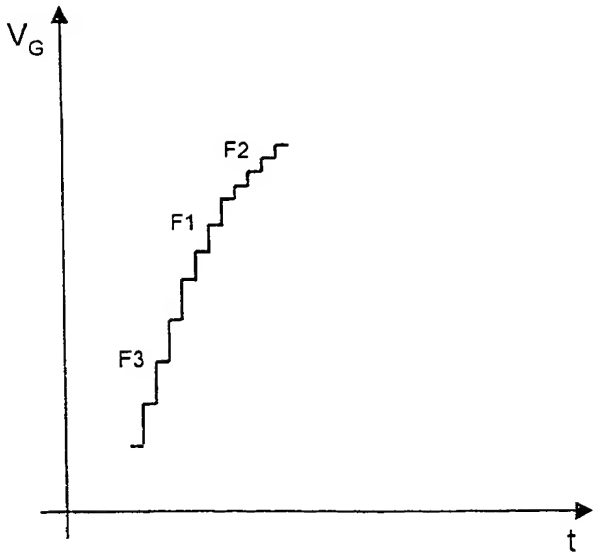


Fig.6a

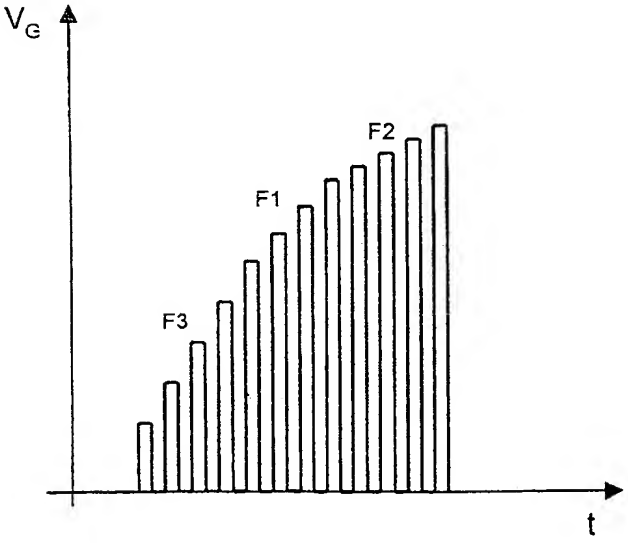


Fig.6b

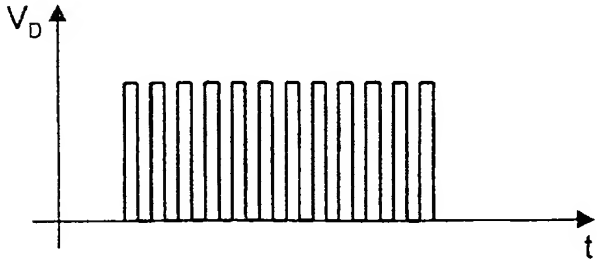


Fig.6c

Pulse No.	Error on threshold voltage variation ΔV_T
$n + 1$	$(1 - \gamma)(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
$n + 2$	$(1 - \gamma)^2(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
$n + 3$	$(1 - \gamma)^3(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
$n + 4$	$(1 - \gamma)^4(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
$n + 5$	$(1 - \gamma)^5(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
⋮	⋮
$n + i$	$(1 - \gamma)^i(\Delta V_{G1} - \Delta V_{G2})/\Delta V_{G2}$
⋮	⋮

Table I

Fig. 7

Pulse No.	ΔV_G [mV]	Threshold voltage variation ΔV_T			
		γ = 0.6	γ = 0.7	γ = 0.8	γ = 0.9
N	400.000	400.000	400.000	400.000	400.000
n + 1	100.000	220.000	190.000	160.000	130.000
n + 2	100.000	148.000	127.000	112.000	103.000
n + 3	100.000	119.200	108.100	102.400	100.300
n + 4	100.000	107.680	102.430	100.480	100.030
n + 5	100.000	103.072	100.729	100.096	100.003
n + 6	100.000	101.229	100.219	100.019	100.000
n + 7	100.000	100.492	100.066	100.004	100.000
n + 8	100.000	100.197	100.020	100.001	100.000
n + 9	100.000	100.079	100.006	100.000	100.000
n + 10	100.000	100.031	100.002	100.000	100.000

Table II

Fig. 8

Pulse No.	Percentage error on threshold voltage variation ΔV_T			
	$\gamma = 0.6$	$\gamma = 0.7$	$\gamma = 0.8$	$\gamma = 0.9$
$n + 1$	120.000000	90.000000	60.000000	30.000000
$n + 2$	48.000000	27.000000	12.000000	3.000000
$n + 3$	19.200000	8.100000	2.400000	0.300000
$n - 4$	7.680000	2.430000	0.480000	0.030000
$n + 5$	3.072000	0.729000	0.096000	0.003000
$n + 6$	1.228800	0.218700	0.019200	0.000300
$n + 7$	0.491520	0.065610	0.003840	0.000030
$n + 8$	0.196608	0.019683	0.000768	0.000003
$n + 9$	0.078643	0.005905	0.000154	0.000000
$n - 10$	0.031457	0.001771	0.000031	0.000000

Table III

Fig. 9

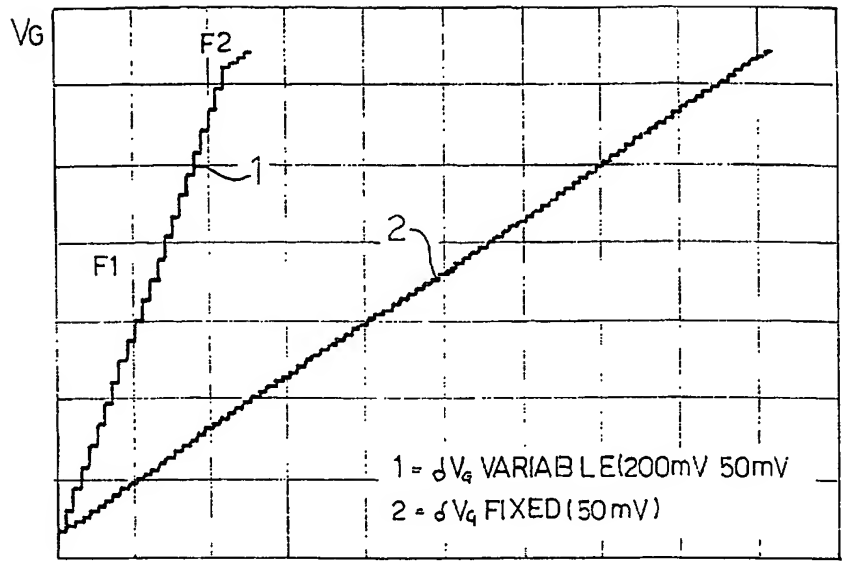


Fig.10a

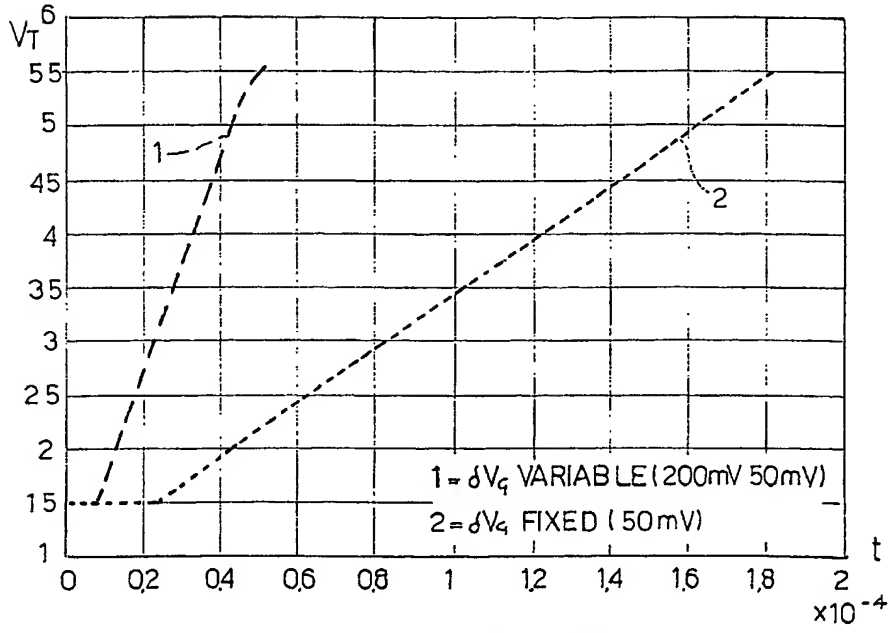


Fig.10b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 83 0247

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X,D	US 5 812 457 A (ARASE KENSHIRO) 22 September 1998 (1998-09-22) * abstract; claims 1,2; figures 2,5,8,10 *	1,13	G11C16/12
Y	US 5 258 949 A (CHANG KO-MIN ET AL) 2 November 1993 (1993-11-02) * column 5, line 47 - column 6, line 29; figure 4 *	1,6,13	
Y	US 4 628 487 A (SMAYLING MICHAEL C) 9 December 1986 (1986-12-09) * column 3, line 55 - column 4, line 61; figure 4 *	2	
Y	US 5 774 397 A (ARITOME SEIICHI ET AL) 30 June 1998 (1998-06-30) * column 25, line 10 - line 23; figure 24A *	1,2,6,13	
A	US 6 034 895 A (NAURA DAVID ET AL) 7 March 2000 (2000-03-07) * column 2, line 20 - line 60; figure 2 *	1-14	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G11C
D,A	US 5 257 225 A (LEE ROGER R) 26 October 1993 (1993-10-26) * the whole document *	1	
D,A	US 4 357 685 A (MAGRUCCI ALDO ET AL) 2 November 1982 (1982-11-02) * abstract; figures 6A,6B *	1	
A	DE 100 34 743 A (SAMSUNG ELECTRONICS CO LTD) 15 February 2001 (2001-02-15) * column 3, line 15 - column 5, line 12; figures 3,4 *	1	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 September 2001	WOLFF, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 83 0247

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

04-09-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5812457 A	22-09-1998	JP 10083686 A	31-03-1998
		JP 10083688 A	31-03-1998
US 5258949 A	02-11-1993	JP 4285795 A	09-10-1992
US 4628487 A	09-12-1986	JP 1935474 C	26-05-1995
		JP 6066475 B	24-08-1994
		JP 61184797 A	18-08-1986
US 5774397 A	30-06-1998	JP 7169284 A	04-07-1995
		US 5946231 A	31-08-1999
		US 6014330 A	11-01-2000
		DE 4422810 A	30-03-1995
		JP 7073688 A	17-03-1995
		KR 135701 B	15-05-1998
		US 5555204 A	10-09-1996
		US 6188611 B	13-02-2001
US 6034895 A	07-03-2000	FR 2738386 A	07-03-1997
		DE 69600963 D	17-12-1998
		DE 69600963 T	01-04-1999
		EP 0762428 A	12-03-1997
		US 5883833 A	16-03-1999
US 5257225 A	26-10-1993	NONE	
US 4357685 A	02-11-1982	IT 1224062 B	26-09-1990
		DE 3036375 A	16-04-1981
		FR 2466834 A	10-04-1981
		GB 2062388 A	20-05-1981
DE 10034743 A	15-02-2001	CN 1282077 A	31-01-2001
		FR 2798218 A	09-03-2001
		JP 2001052486 A	23-02-2001
		US 6212101 B	03-04-2001

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/001232

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 926 409 A (ENGH ET AL) 20 July 1999 (1999-07-20) column 1, line 14 - column 2, line 40	1-12, 20-35
A	US 6 301 161 B1 (HOLZMANN PETER J ET AL) 9 October 2001 (2001-10-09) cited in the application the whole document	1-12, 20-35
X	EP 1 249 842 A (STMICROELECTRONICS S.R.L) 16 October 2002 (2002-10-16) paragraph '0024! - paragraph '0066!	13,14, 18,19, 36,38,39

Vierra Magen Marcus Harmon & DeNiro
File: 1--SAND-01011US0
Action: IDS from PCT
Due Date: November 5, 2005
Final Due Date:
Atty: JM Dkt: Verify

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 July 2005	05. 08. 2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Harms, J

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/001232

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 220 531 A (BLYTH ET AL) 15 June 1993 (1993-06-15) cited in the application column 4, line 39 - column 6, line 14; figure 2 -----	13,36
X	US 2002/024846 A1 (KAWAHARA TAKAYUKI ET AL) 28 February 2002 (2002-02-28) paragraph '0018! paragraph '0149! - paragraph '0167!; figures 1-3 -----	13,14, 18,19, 36,38,39

4

Form PCT/ISA/210 (continuation of second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US2005/001232

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5926409 A	20-07-1999	NONE	
US 6301161 B1	09-10-2001	CA 2344791 A1	25-10-2001
		EP 1154439 A1	14-11-2001
		JP 2001357693 A	26-12-2001
EP 1249842 A	16-10-2002	EP 1249842 A1	16-10-2002
		JP 2002319293 A	31-10-2002
		US 2002191444 A1	19-12-2002
US 5220531 A	15-06-1993	CA 2099500 A1	03-07-1992
		DE 69131205 D1	10-06-1999
		DE 69131205 T2	30-09-1999
		EP 0565622 A1	20-10-1993
		JP 6504156 T	12-05-1994
		JP 3111386 B2	20-11-2000
		KR 155575 B1	01-12-1998
		SG 46535 A1	20-02-1998
		WO 9212519 A1	23-07-1992
US 2002024846 A1	28-02-2002	JP 10106276 A	24-04-1998
		US 6459621 B1	01-10-2002
		US 2001000023 A1	15-03-2001
		US 6163485 A	19-12-2000
		US 6134148 A	17-10-2000
		US 6091640 A	18-07-2000